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RESEARCH DEPARTMENT

REPORT

Pulse code modulation for high-quality sound signal distribution: Instrumentation of experimental multiplex system

No. 1970/36

Research Department, Engineering Division
THE BRITISH BROADCASTING CORPORATION

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PULSE-CODE MODULATION FOR HIGH-QUALITY SOUND-SIGNAL DISTRIBUTION: INSTRUMENTATION OF EXPERIMENTAL MULTIPLEX SYSTEM

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Summary

A description is given of experimental equipment constructed to test the feasibility of p.c.m. multiplex transmission of a number of high-quality mono or stereo sound-signals.

Using currently available electronic components it was found possible, without undue difficulty, to achieve 14-bit coding at sampling frequencies up to 38 kHz and to produce a multiplex signal at 8 Mb/s; these parameters cover the most stringent requirements to be expected in practice.

1. Introduction

In carrying out the study of p.c.m. time-division multiplex applied to high-quality sound signals, the general features of which are dealt with in an earlier report[1], experimental equipment was built. The present report deals with the methods adopted to achieve the required performance, and with such of the instrumental details as are thought to be interesting or novel.

2. Analogue-to-digital and digital-to-analogue converters

The ramp counter method of analogue-to-digital conversion (coding), in which the output number is accumulated in a counter during the time when a ramp voltage is rising to equality with the input signal, has been found very suitable for coding sound signals with a precision of up to 11 bits.[2]

The inverse process, in which a ramp accumulates voltage during the period in which an input number is being counted out, was found equally suitable for digital-to-analogue conversion (decoding) of sound signals to the same precision.

2.1. Coding

For reasons given in the earlier report[1], the experimental equipment was required to code signals to 14-bit accuracy at a repetition rate of 38 kHz. To use the simple ramp-counter method would have meant impracticably high counting speeds – of the order of 640 MHz.

In the experimental coder, a modification of the ramp-counter technique is therefore used. The quantum levels are considered to be in groups, each group containing a fixed number of units. In counting out the levels whole groups are counted first, after which the coder 'changes gear' and counts the remaining units. By this coarse-and-fine method of coding, the number of counting operations required is greatly reduced and the necessary counting frequency is only 15 MHz.

To code signals to 14-bit precision, the 2^{14} quantum levels are grouped into 2^8 (256) groups, each

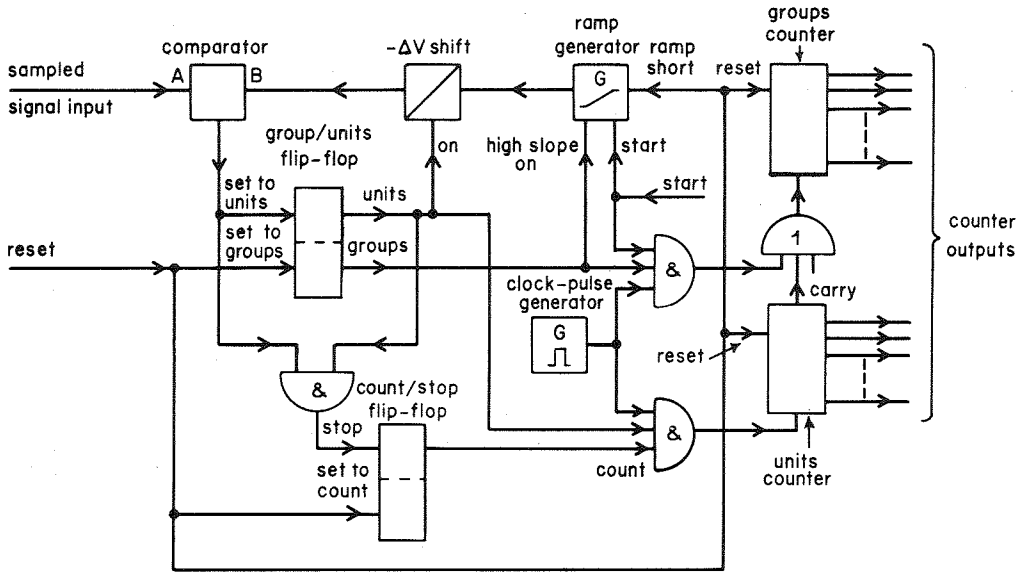

Fig. 1 — Coder conversion equipment schematic diagram

containing 2^6 (64) units. Fig. 1 shows a schematic diagram of the part of the coder directly concerned with the conversion process. To convert each sample the ramp is first set to a high slope which traverses 1/256 of the total voltage range for each cycle of the counter clock. When the ramp voltage becomes equal to the sample voltage, the comparator stops the counter, and at the next clock pulse the ramp voltage is reduced by an amount appropriate to one group while the ramp slope is reduced by a factor of 64.

At this point, the ramp voltage is that corresponding to the whole number of groups next below the signal sample, and the ramp slope is equal to 1 unit per clock pulse. Conversion is then completed by counting out the remaining units, and the process is finally halted by the comparator when ramp and signal again become equal.

In practice, because of transient effects on the ramp caused by the abrupt change of slope and by the voltage step, it is convenient to make the step larger than 1 group and to compensate for this by initially setting the units section of the counter to a corresponding negative number. By this means, a short time interval is provided while the negative number is being counted out, during which the transient effects die away and the ramp settles down to a steady slope.

There are a number of possible variants in the change-gear mechanism; a combination of rising and falling ramps may be used, while the voltage step at the transition may be added to the signal rather than subtracted from the ramp. The arrangement used here however permits the comparator to make both decisions with voltage changes in the same direction, thus avoiding any hysteresis effects. The choice of two rising ramps also permits good thermal tracking of the ramp currents since these may be supplied from a common power rail via a pair of thermally coupled transistors.

The method of locking the coder and decoder to the repetition frequency of the multiplexing equipment is identical to that employed in synchronising coders to television and described in an earlier report.[3]

2.2. Decoding

In the decoder, the digital signal is again dealt with in groups and units, corresponding to coarse and fine steps in the analogue signal; in this case, the output for both groups and units in the incoming code can be accumulated simultaneously. Fig. 2 shows a schematic diagram of the part of the decoder directly concerned with conversion. The digital signal to be converted to analogue form is preset into the two sections (groups and units) of a run-down counter. Counting is commenced and simultaneously the ramp generator is started. In the ramp generator two currents are applied to a single integrating capacitor; the larger of the currents, controlled by the groups counter, produces a fast rise — 1/256 of the total range for each clock pulse — while the smaller current, controlled by the units counter, produces a slow rise — 1/64 of the other. Each current is stopped when the counter controlling it reaches zero. When both have done so the voltage on the capacitor is proportional to the input number. This voltage is then sampled and filtered to re-create the original audio signal.

3. The multiplexer

The experimental multiplex equipment was designed to be capable of transmitting 13 monophonic sound channels together with two additional channels required for error detection and framing. These fifteen channels, each having fourteen bits per word, repeated at 26·3μs intervals (38 kHz sampling), require a data rate of 7·98 Mb/s.

The data is sent to line as a continuous stream and therefore the time slot for each bit is 125·3 ns wide. To minimise timing differences within the

multiplex, the propagation delays of the digital integrated circuits handling the data were required to be small compared with the 125 ns slot, and emitter-coupled logic with a propagation delay of about 6 ns per gate was chosen.

Fig. 3 shows a schematic diagram of the multiplexer. The complete cycle of multiplex operation, during which a 'frame' of 15 channels (210 bits) is transmitted, is controlled by the bit-rate clock and the associated bit and word counters.

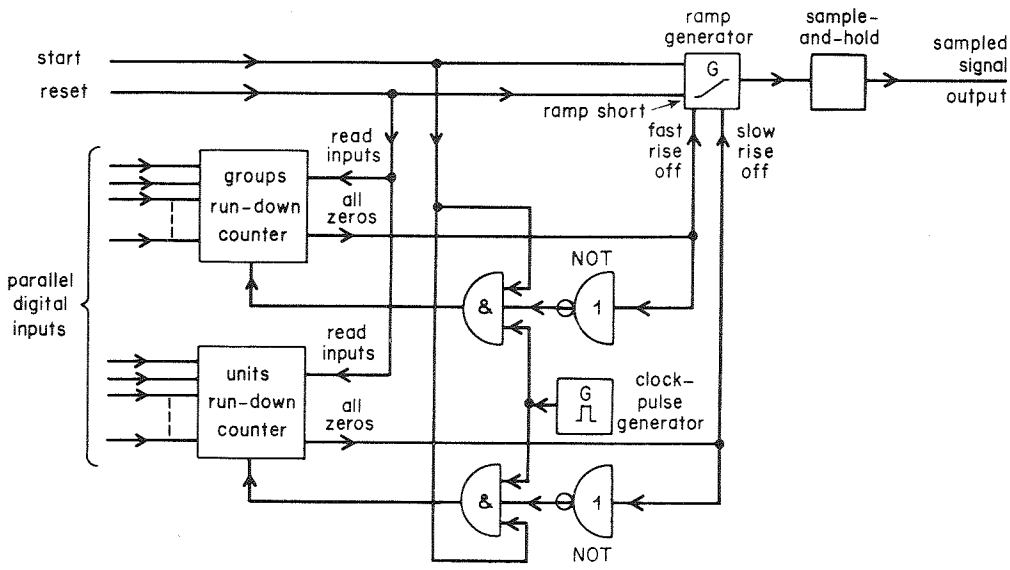

Fig. 2 – Decoder conversion equipment schematic diagram

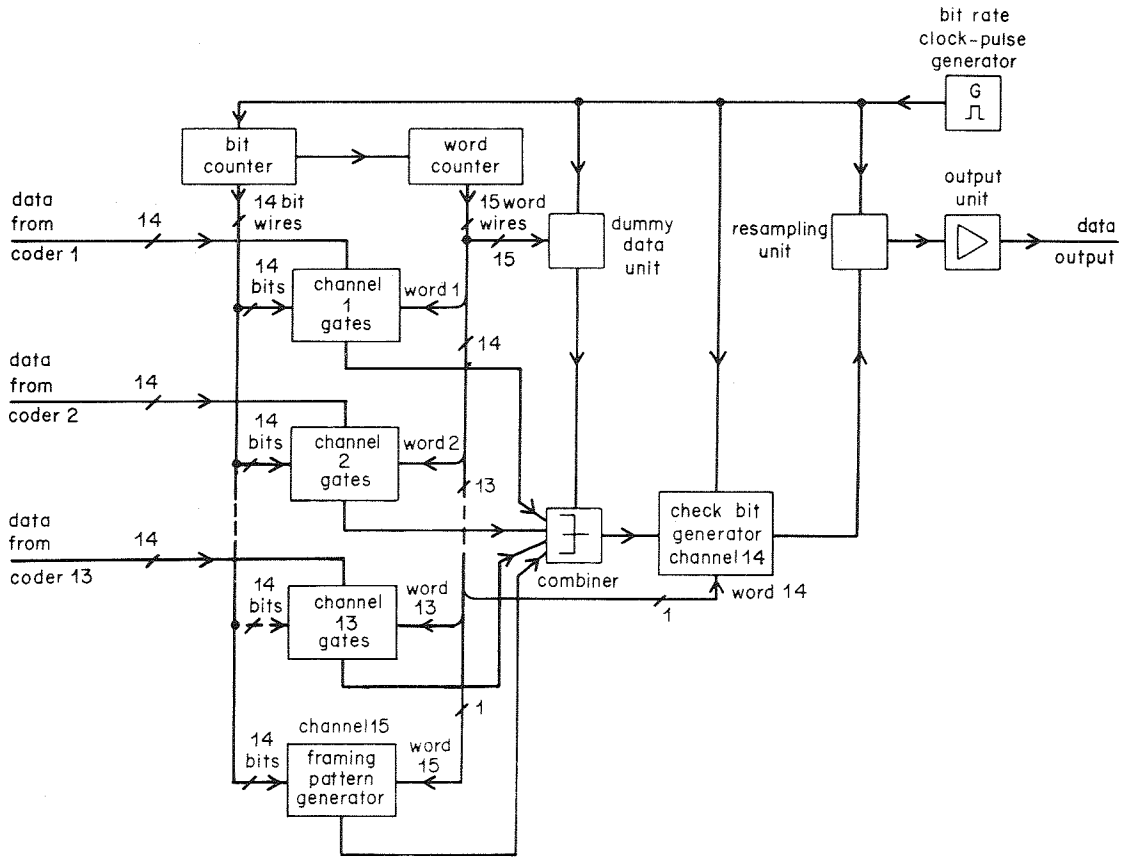

Fig. 3 – Multiplexer schematic diagram

The counters are of the 'twisted ring' type.[4] This configuration was chosen because of the simplicity with which the states can be decoded. The bit counter counts the bits in each channel word; after the fourteenth bit it moves the word counter on by one unit, and then repeats the process. Fifteen states are obtained from the word counter by using an eight-stage (16-state) circuit and using a 'knock on' pulse to bypass one state.

Each sound channel coder presents its output as parallel digits continuously available on fourteen separate wires. These digits are gated into the appropriate time slots under the control of the pulses from the bit and word counters. Each gate is unlocked by the word pulse for that channel and opened by the bit pulse at the proper moment.

The block of data containing one word from each of the thirteen programme channels is then fed to a digit generator which inserts error detection (check) digits in channel 14. To the resulting block of 14 channel words is added a framing pattern in channel 15.

Before sending the output pulses to line, any timing errors due to differential propagation delays in the various paths of the multiplex are removed by resampling the data at the mid-point of each bit time slot. On resampling, a narrow pulse (30 ns) is generated for each data '1' and a filter then converts these narrow spikes into (cosine)^2 pulses with a half-height duration of 125 ns, occupying a bandwidth of 8 MHz.

In order to provide additional synchronising information for the receiving terminal equipment when only a few channels are in use, dummy data is inserted in the unused channels. This is easily achieved by dividing down the output of the sending terminal bit rate clock. In the present case the clock frequency is divided by four and the resulting dummy data consists of a repetition of two ones followed by two zeros.

4. The demultiplexer

Fig. 4 shows the schematic diagram of the demultiplexer. Zero crossings of the incoming data are used to synchronise the bit-rate clock. To find these zero crossings the mid-point of the incoming data swing must first be located; this is done by measuring both positive- and negative-going peaks of the pulses by means of peak rectifiers in the input unit and deriving the mean of the rectified voltages. The mean voltage is applied to one input of a comparator and the incoming data to the other; the comparator output then consists of amplitude-limited pulses with the original data zero crossings preserved.

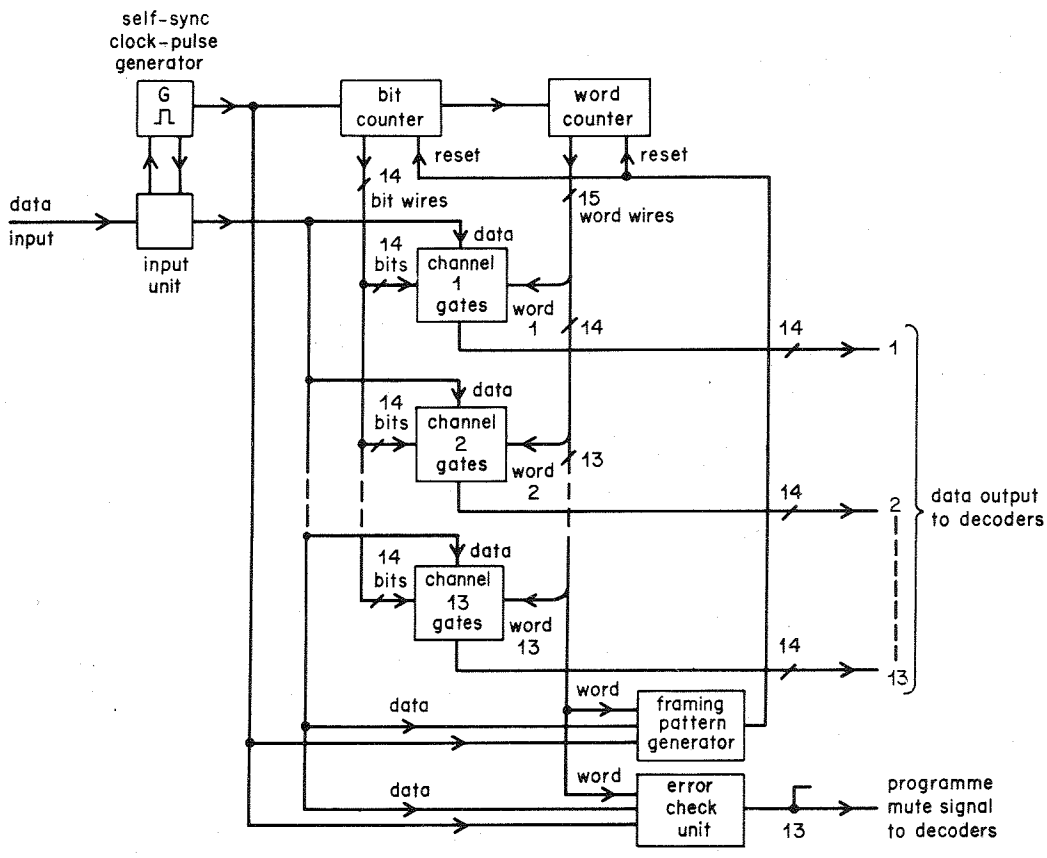

Fig. 4 – Demultiplexer schematic diagram

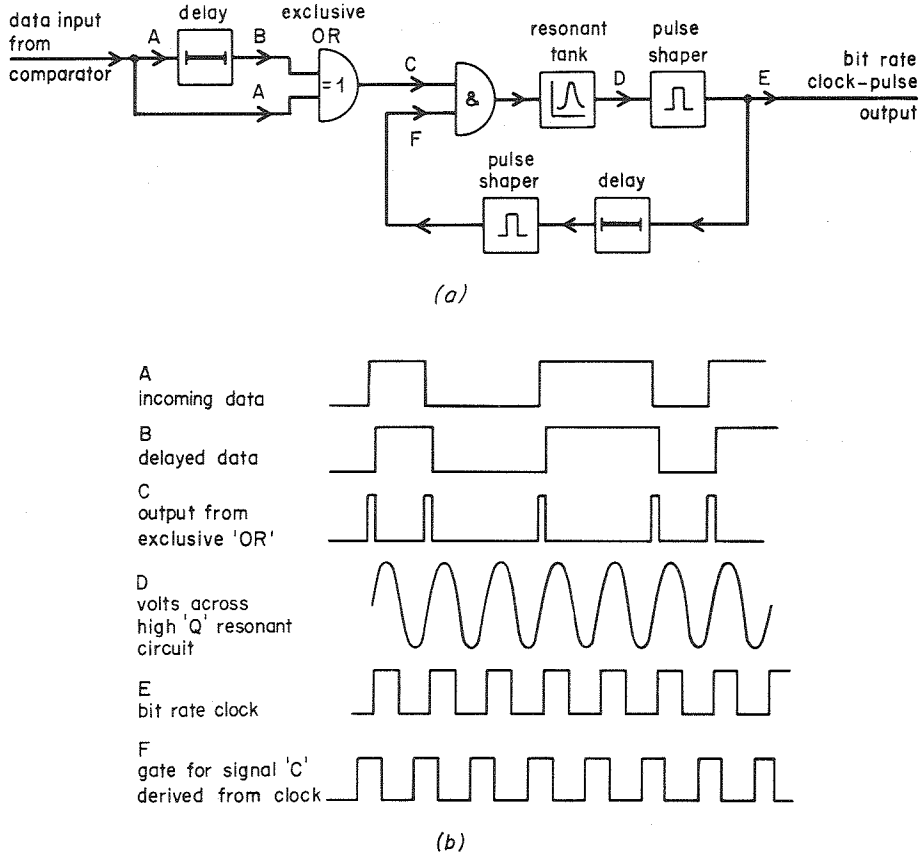

Fig. 5 — Bit rate clock
(*a*) schematic diagram (*b*) timing diagram

The data pulses from the comparator output are used to derive bit-rate clock pulses to operate all the other units of the demultiplexer. Fig. 5 shows the schematic and timing diagrams of the bit-rate clock. Short pulses commencing at the zero crossings of the data are derived by applying data to one input of an exclusive OR gate and the same data, delayed by a few gate propagation delays, to the other. These short pulses are applied as current impulses to a high Q resonant tank circuit. The resulting sinusoidal voltage waveform at the terminals of the tank circuit is reshaped as a square wave and then serves as a bit-rate clock.

When the timing of the data zero crossings is disturbed by severe noise on the link the clock amplitude and phase are both disturbed and the data may be lost due to clock failure. The situation is greatly improved by deriving gating pulses F from the clock output so that those pulses in signal C which are widely divergent from the expected timing are eliminated.

The channel separation switches which route the data to the correct decoder terminals are AND gates as in the multiplexer and are similarly controlled by pulses from bit and word counters. After synchronism of the clock as described above has been achieved, frame synchronism is next required. At the end of each transmitted frame of data the framing pattern will be received. To achieve frame synchronism the data is clocked through a shift register in the framing pattern detector and the data in all stages of the shift register is continually scrutinised by a fourteen-input digital comparator programmed to accept only the framing pattern. When the framing pattern has completely filled the shift register, the digital comparator produces an output pulse which is used to reset both the word and bit counters ready for the first pulse of the next frame. After the comparator output pulse has appeared and frame synchronisation has occurred, the input of data to the shift register is interrupted until the next pattern is expected, thus preventing misframing of the demultiplex by framing patterns generated fortuitously in the message.

Reframing upon receipt of an incorrect pattern is deferred by the action of a counter until four such patterns have been received in succession: this precaution reduces the number of attempted reframings caused by patterns spoiled by interference on the transmission link when bit synchronism is still adequate. The time taken to restore synchronism is about 0·1 ms.

5. Error detection

Investigation of error detection, concealment and correction is being undertaken as a separate study, the results of which will appear in a later report.

6. Conclusions

Experimental equipment to perform the necessary coding, multiplexing, demultiplexing and decoding operations has been developed for a high-quality sound distribution system working in p.c.m.

Although the system parameters had been chosen to include the most challenging conditions which might be met in an operational system, the instrumental requirements which arose could all be satisfied using commercially available integrated circuits and discrete components. No areas of outstanding instrumental difficulty have appeared which could seriously hamper the design of future operational equipment.

7. References

1. Pulse-code modulation for high-quality sound-signal distribution: feasibility of multiplex system. BBC Research Department Report in course of preparation.

2. Pulse-code modulation for high-quality sound-signal distribution: coding and decoding. BBC Research Department Report No. EL-18, Serial No. 1968/29.

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